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EXAMINER	
PARK, ILWOO	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,611	MARTWICK, ANDREW W.	
	Examiner	Art Unit	
	Ilwoo Park	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-19,21-29* is/are rejected.

7)☒ Claim(s) *10,20 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are presented for examination. Cooper et al., Estakhri et al., and Tanaka et al. were cited in the last office action.

Terminal Disclaimer

2. The terminal disclaimer filed on 1/27/2005 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US patent No. 6,718,407 has been reviewed and is NOT accepted.

The terminal disclaimer does not comply with 37 CFR 1.321(b) and/or (c) because the application/patent being disclaimed has not been identified.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-18 of U.S. Patent No. 6,718,407 contain every element of claims 1-30 of the instant application and as such anticipate claims 1-30 of the instant application. "A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896,

225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). "ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Court, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 11, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper et al., US patent No. 5,805,882 in view of Estakhri et al., US patent No. 5,606,660.

As to claims 1 and 11, Cooper et al teach a method and an apparatus comprising:

receiving [col. 11, lines 19-37] a programming information to update [col. 3, lines 18-26] a firmware device [flash ROM 122], separated from a processor, containing a boot code [col. 5, lines 32-35; col. 9, lines 48-52] for the processor from a communication interface [parallel port 180]; and

parsing [col. 11, lines 19-37; fig. 10B] the programming information into control commands and program data by a parser. Cooper teaches a firmware device [flash ROM 122] and a chipset [MSIO 120] and Estakhri teaches a firmware device [RAM 320, ROM 330] and a chipset [controller semiconductor chip 300]

Though, Cooper et al teach a firmware device and a chipset [MSIO 120], Cooper et al do not teach the firmware device is in the chipset. Estakhri et al teach a firmware device [e.g., RAM 320, ROM 330] containing a boot code [col. 3, lines 26-33] for a processor [microprocessor 500] in a chipset [controller 300].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Cooper et al and Estakhri et al because they both teach a firmware device and a chipset and the Estakhri et al's teaching of a firmware device included in a chipset would increase efficiency by reducing space [Estakhri et al: col. 1, lines 15-22; col. 3, lines 1-2] of Cooper et al's portable computer.

6. As to claim 21, Cooper et al teach a system comprising:

a processor [CPU 100];

a firmware device [flash ROM 122]; and

a self-update firmware controller [mobile super I/O 120] coupled to the firmware device to self update [col. 3, lines 18-26] the firmware device, the controller comprising:

a communication interface to receive [col. 11, lines 19-37] programming information to update the firmware device, separated from the processor, containing a boot code [col. 5, lines 32-35; col. 9, lines 48-52] for the processor, and

a parser coupled to the communication interface to parse [col. 11, lines 19-37; fig. 10B] the programming information into control commands and program data.

Though, Cooper et al teach a firmware device and a chipset [MSIO 120], Cooper et al do not teach the firmware device is in the chipset. Estakhri et al teach a firmware device [e.g., RAM 320, ROM 330] containing a boot code [col. 3, lines 26-33] for a processor [microprocessor 500] in a chipset [controller 300].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Cooper et al and Estakhri et al because they both teach a firmware device and a chipset and the Estakhri et al's teaching of a firmware device included in a chipset would increase efficiency by reducing space [Estakhri et al: col. 1, lines 15-22; col. 3, lines 1-2] of Cooper et al's portable computer.

7. Claims 2-9, 12-19, and 22-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper et el and Estakhri et al as applied to claims 1, 11, and 21 above, and further in view of Tanaka et al., US patent No. 6,266,810.

As to claims 2, 12, and 22, Cooper et al and Estakhri et al teach programming the firmware device based on the control commands by control logic circuit [mobile super I/O 120 of Cooper et al]. However, Cooper et al and Estakhri et al do not explicitly disclose a buffer to store the program data to be written into the firmware device.

Tanaka et al teach a buffer [col. 4, lines 40-45] to store a program data to be written into a firmware device [flash ROM 101].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the Tanaka et al's teaching of the buffer to store the program data to be written into the firmware device in order to increase flexibility in timing for programming the firmware device of Cooper et al and Estakhri et al.

8. As to claims 3, 13, and 23, Cooper et al teach providing the programming information to the parser by a source selector [fig. 2; col. 7, lines 38-54].

9. As to claims 4, 14, and 24, Cooper et al teach selecting one of the programming information [col. 7, lines 38-54] from the communication interface and an input and output (I/O) channel data [col. 7, lines 41-44] by a multiplexor [multiplexor 178].

10. As to claims 5, 15, and 25, Cooper et al teach erasing [col. 13, lines 51-54] the firmware device by an erase control circuit and Tanaka teaches writing [col. 4, lines 35-39] to the firmware device using the program data in the buffer by a write control circuit.

11. As to claims 6, 16, and 26, Cooper et al teach generating the control commands based on the parsed programming information by a state machine [col. 11, lines 19-37; fig. 10B], the control commands including [col. 13, lines 46-54] at least an erase command and a write command.

12. As to claims 7, 17, and 27, Cooper et al teach the programming information includes at least a self-update identifier [col. 12, line 61-col. 13, line 3], program parameters [col. 14, lines 6-8], and program data [col. 14, lines 15-16].

13. As to claims 8, 18, and 28, Cooper et al teach recognizing [col. 12, line 61-col. 13, line 3] the self-update identifier, reading [col. 14, lines 6-8] the program parameters including at least erase, and write addresses and generating an erase command to the

erase control circuit to a block [col. 13, lines 20-32] in the firmware device at the erase address, and Tanaka et al teach generating a buffer write command to write [col. 4, lines 40-45] the program data into the buffer and generating a write command to the write control circuit to the program data in the buffer to the firmware device at the write address [col. 4, lines 35-39].

14. As to claims 9, 19, and 29, Cooper et al and Estakhri et al do not disclose converting serial data [packet] into the programming information by a serial to parallel converter; in fact, Cooper et al and Estakhri et al teach receiving the programming information in parallel form through the parallel communication interface. Tanaka et al implicitly teach converting serial data [packet stream] into the programming information by a serial to parallel converter. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include Tanaka et al's teaching of receiving and converting serial data into the programming information by a serial to parallel converter in order to increase flexibility by adapting prevalent serial interface.

Allowable Subject Matter

15. Claims 10, 20, and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

16. Applicant's arguments filed 1/27/2005 have been fully considered but they are not persuasive. Applicant argues in substance that **a)** there is no teaching or suggestion

that a chipset separated from the processor is present or **b)** there is no motivation to combine Cooper, Estakhri, and Tanaka because none of them addresses the problem of updating a firmware device in a chipset separated from the processor.

For the point **a)**, Estakhri at least teaches a chipset [controller semiconductor chip 300 in fig. 6] separated from the processor [microprocessor 500]. Further, Estakhri at least teaches a firmware device [e.g., RAM 320, ROM 330] containing a boot code [col. 3, lines 26-33] in the chipset for the processor.

For the point **b)**, Cooper teaches a firmware device [flash ROM 122] and a chipset [MSIO 120] and Estakhri teaches a firmware device [RAM 320, ROM 330] and a chipset [controller semiconductor chip 300]; Estakhri addresses cost and space problem [col. 1, lines 15-30] if the firmware device is separated from the chipset and solves the problem by embedding the firmware device into the chipset [fig. 6]. Thus, one of ordinary skill in the art could be easily motivated by Estakhri's teaching of embedding the firmware device into the chipset rather than separating the firmware device from the chipset in order to save cost and space.

Further, combination of Cooper and Estakhri teaches receiving a program data and directly programming the data into the firmware device without buffering the data; specifically, a flash programming protocol of Cooper strictly shows receiving each byte of a programming data transmitted through a communication interface from a host, writing the data byte directly into the flash ROM, receiving next data byte from the interface, writing the next data byte into the flash ROM, repeatedly until byte count reaches to zero. Speed of programming of a flash ROM and a speed of data

transmission through the communication interface are dependent each other. In other words, if the parallel communication interface has a higher data transmission speed than the speed of programming of the flash ROM, the data transmission speed cannot go higher. Tanaka teaches receiving a program data, buffering the data into a buffer before programming, and programming the data into the firmware device. Thus, one of ordinary skill in the art at the time the invention was made already recognizes that the buffer of Tanaka could enable operations of the communication interface and programming independently or enable to maximize the data transmission speed and programming in convenient time.

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ilwoo Park whose telephone number is (571) 272-4155.

The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (571) 272-4146. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ILWOO PARK
PRIMARY EXAMINER

Ilwoo Park
June 08, 2005